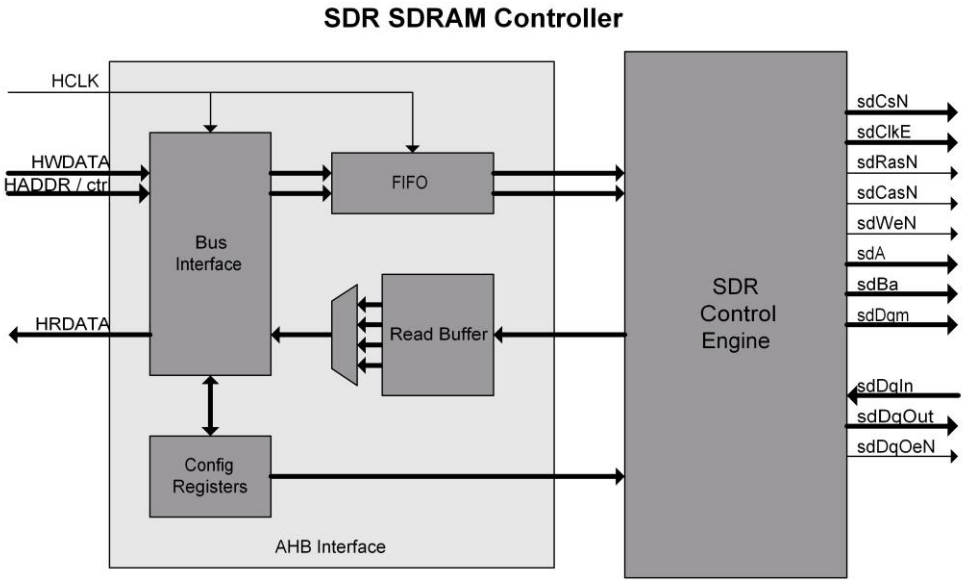
SDRAM Control IP Core

IPC-SDRamCtrl-AHB

Features

- AMBA® AHB Compatible
- Controls up to 256MB SDRAM
- Handles AHB Burst modes



Overview

The SDRAM Controller provides the interface between external SDRAM devices and an AHB system bus. This controller can control quad-bank SDRAM devices up to 256MB. The controller has several configuration options for compatibility with a wide variety of devices. Requests from the AHB bus are passed on to the control engine which handles device initialization, refresh, and read/write accesses to memory. Accesses to SDRAM always occur in bursts of 4. A FIFO is used to pass read/write instructions to the control engine and a read buffer is used to reduce read latency and improve performance.

The AHB interface allows bus masters on the AHB bus to communicate to the SDRAM through the SDRAM control engine and can respond with one of two following slave transfer responses, OKAY and ERROR.

All types of burst transfers defined by the AMBA specification are supported. These include single beat, fixed-length incremental, fixed-length wrapping, and undefined-length incremental transfers. Early burst termination is also supported.

The licensed IP package includes:

Verilog Source
Complete Verilog Test Environment
Simulation and synthesis scripts

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You may also be interested in:

Low Power Subsystem
Low Power / Performance Subsystem
Custom Performance Subsystem

Infrastructure Cores

AHB Multi-Matrix Fabric
AHB/AHBLite Channel
AHB Arbiter
AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AHB to ABP Bridge
APB Channel

AXI Cores

AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AXI External Bus Interface
(Memory/Flash Controller)
AXI Internal Memory Controller

AHB Cores

AHB Channel
AHB Multi-Matrix Fabric
AHB to ABP Bridge
AHB Arbiter
AHB QSPI with Execute in Place (XIP)
AHB External Bus Interface
AHB Internal SRAM Controller
AHB Interrupt Controller
AHB DMA Controller
AHB DMA 4 Channel Controller
AHB TFT LCD Controller
AHB DES/TDES Encryption/Decryption

APB Cores

APB Channel
APB Quad SPI Controller
APB General Purpose IO
APB Timer
APB UART
APB I2C (Master and Slave)
APB SPI
APB Watchdog Timer
APB Pulse Width Modulator
APB Real Time Clock
APB Parallel Port
APB Remap (for boot)

General

DES/TDES – Digital Encryption Standard

For more information contact

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