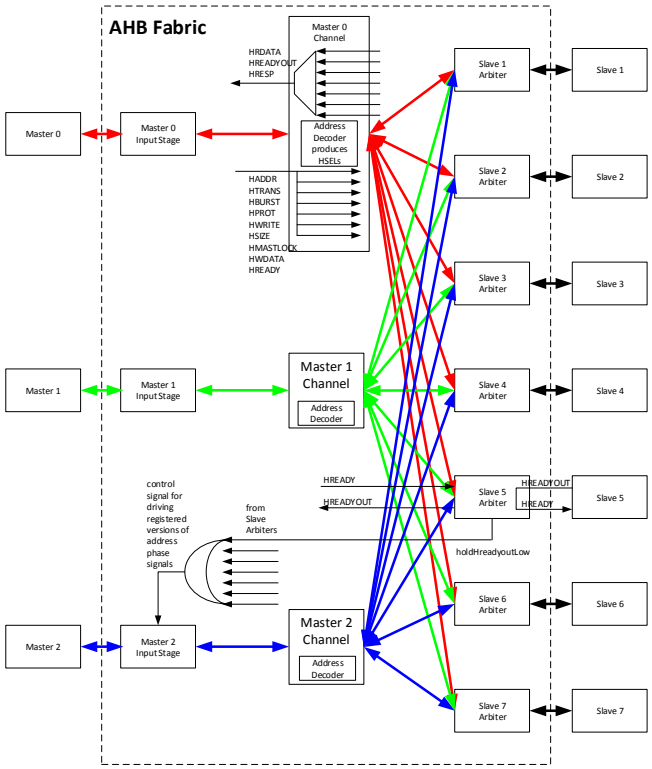
AHB Multilayer Fabric IP Core
IPC-MultiMatrix-AHB

Features

- AMBA® 2.0 Compatible
- 4 AHB Channels
- Supports 4 Masters and up 7 Slaves
- Arbitration is done at each slave
- Easily expandable



Overview

The AHB Fabric provides the necessary infrastructure to connect as many as 7 shared AHB Slaves (numbered 1-7) to as many as 3 AHB-Lite Bus Masters. In a typical AHB system, several AHB Masters may compete for a shared (AHB) bus; a bus arbiter determines bus ownership. The AHB Fabric allows for the various AHB-Lite Masters to connect to several different shared peripherals without the need to arbitrate for a shared AHB bus. Instead, arbitration is performed at the peripheral. This way, the various Masters may see a significant increase in performance over a standard AHB system. However, systems where multiple masters need frequent access to the SAME peripheral will see only a modest performance increase.

The AHB Fabric may be used as either a partial or a complete AHB-Lite subsystem. That is, it may be used in a standalone fashion to comprise a complete AHB subsystem, or in conjunction with an AHB Channel module as part of a larger AHB subsystem. If used in conjunction with an AHB Channel, because both the Fabric and the Channel perform address decoding, it is important that the decoded address space for the Fabric be mutually exclusive to that of the AHB Channel.

The Fabric may be connected to the remainder of the subsystem as follows. Each of the AHB Fabric's 7 Mirrored Slave Ports is connected to an AHB Slave module (e.g. External Bus Interface, Memory Controller, AHB-to-APB Bridge). On the Master side, each of the 3 AHB Fabric's Mirrored Master Ports is connected to either the output side of an AHB Arbiter (in the case where each AHB system has multiple bus Masters) or directly to an AHB or AHB-Lite Master such as a micro-processor.

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AHB Multilayer Fabric IP Core
IPC-MultiMatrix-AHB

The licensed IP package includes:

Verilog Source
Complete Verilog Test Environment
C-Sample Code:

You may also be interested in:

Low Power Subsystem
Low Power / Performance Subsystem
Custom Performance Subsystem

Infrastructure Cores

AHB Multi-Matrix Fabric
AHB/AHBLite Channel
AHB Arbiter
AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AHB to ABP Bridge
APB Channel

AXI Cores

AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AXI External Bus Interface
(Memory/Flash Controller)
AXI Internal Memory Controller

AHB Cores

AHB Channel
AHB Multi-Matrix Fabric
AHB to ABP Bridge
AHB Arbiter
AHB QSPI with Execute in Place (XIP)
AHB External Bus Interface
AHB Internal SRAM Controller
AHB Interrupt Controller
AHB DMA Controller
AHB DMA 4 Channel Controller
AHB TFT LCD Controller
AHB DES/TDES Encryption/Decryption

APB Cores

APB Channel
APB Quad SPI Controller
APB General Purpose IO
APB Timer
APB UART
APB I2C (Master and Slave)
APB SPI
APB Watchdog Timer
APB Pulse Width Modulator
APB Real Time Clock
APB Parallel Port
APB Remap (for boot)

General

DES/TDES – Digital Encryption Standard

For more information contact

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