Multi-Voltage GPIO with HDMI, LVDS and Analog Pads Library
TSMC 28nm HPM

A 1.8V to 3.3V/0.9V Digital GPIO Library, which includes an HDMI, LVDS and Analog/RF Low capacitance pad set in TSMC N28 HPM process.

FEATURES
- VDDIO = dynamically selectable 1.8V, 2.8V or 3.3V
- VDD = 0.9V
- Dual-row, staggered pitch of 25um
- Cell height 130um, width 25um
- Outer bond pad opening: 44um x 55um y
- Inner bond pad opening: 44 um x 55um y
- Shorted Output Protection
- HBM 3000V
- CDM 800V
- MM 300V
- IE 2kV
- Junction temp range: -40°C to 125°C
- Can integrate with TSMC standard IO

HDMI and LVDS Pad Features

- Are not PHYs, but are bondpads with ESD and Powers
- Includes Power and GND pads
- <250fF per IO including Bondpad
- 1.8V to 3.3V Power supply (HDMI)
- 1.8V Power Supply (LVDS and analog)
- 5V Tolerant (HDMI only)
- Fail-Safe IO (HDMI only)
- Pad Macros provide for ideal parasitic matching between differential signal pins.

- Analog and low-Cap RF pass-through cells (ESD protected)

SUMMARY

The DGIO28HPM pad set has digital cells that can drive spec loads at 25 MHz, 75 MHz, and 150 MHz, allowing you to manage SSI currents and peak power. Digital pads can be configured as input, full output, open source, open drain, with or without an internal 50k ohm pullup or pulldown. Pad cells for IO Power, Ground, Core Power, with built-in ESD circuits are in the set. A key feature is that the VDDIO supplies can be selected and dynamically changed during operation in the system. All digital IO and power pads will detect voltage range and adjust accordingly to meet spec. Allows for a broader customer base with one IO/chip design.

3 Classes of GPIO give designers options for optimizing performance, power and noise
- 150MHz operation for 10pF Loads
- 75 MHz operation for 10pF Loads
- 25 MHz operation for 10pF Loads

Full Speed Output-enable for open drain applications.
- Selectable pull-up or down termination resistors
- Complies with JEDEC JESD 8-5 LVCMOS Specs
- 2kV IEC robust
- Shorted output protection

MODELS and SUPPORT FILES

- GDS Layouts
- LEF Abstracts
- CDL netlist for simulation and LVS
- Liberty Timing files
- Functional models in behavioral Verilog with timing arcs.

FRONT-END DEVICES

- 1.8V Thick-oxide NMOS and PMOS; 0.9V thin oxide NMOS and PMOS and diodes. No ESD Implant layer or special masks required.
- Back-end: Metal1 to Metal8, AP bondpad layer for wirebond, using Circuit-Under-Pad construction.

VARIANTS

- A non-IEC compliant pad set exist that is 110um tall, also has reduced shorted output protection.
- Other variants include special macro cells that allow for alternate bonding package options where the customer can bondout either HDMI/LVDS signals, or GPIO’s. Only sacrifices 60um cell height.
- Can be modified for Flip-Chip applications